REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 19-46 are pending in the present application. Claims 19, 32, 35, 36, 38, and 46 are amended by the present amendment.

Applicant thanks the Examiner for the courtesy of an interview extended to Applicant's representative on October 23, 2009. A clarifying claim amendment, similar to those presented herewith, was discussed. The Examiner kindly indicated that such an amendment would overcome the applied art, and that further searching would be performed. Comments regarding such applied art are included below.

In the outstanding Official Action, Claim 46 was objected due to an informality. Claim 46 has been amended in the manner kindly suggested by the Examiner. Reconsideration and withdrawal of the objection to claim 46 are respectfully requested.

Claims 39-46 were rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement. More specifically, the Official Action states that the "claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention." However, this rejection is respectfully traversed

because the subject matter in Claims 39-46 is respectfully submitted to be supported in the original specification for at least the following reasons.

As regarding Claims 39 and 40, consider for example page 7, lines 6-15 of Applicant's original specification. That portion states in relevant part that "[t]he address identifies the state variable which is to be accessed, the data provides operands which a simple computer uses to modify the variable, and the command 62 selects a locally stored thread of programmed microcode 63 which is able to read, modify and writeback the state variable within a very small number of system clock cycles." Accordingly, it is respectfully submitted that "wherein said operation results in a change of shared state" and "wherein said state engine is a programmable entity capable of executing shared memory instructions" are supported in the originally filed specification.

As regarding Claim 41, consider for example page 3, lines 3-5 of Applicant's original specification. That portion states that "[e]ach said state element means preferably comprises local memory, and each field of a data record is stored in a respective memory of a respective state element means." Accordingly, it is respectfully submitted that "wherein said memory is within said state element" is supported in the originally filed specification.

As regarding Claim 42, consider for example the above quoted portion of page 3, lines 3-5 along with page 8, lines 6-12, which states in relevant part that "[j]ust as atoms are the components of molecules, which may be the building blocks of simple cells, which then combine into simple organisms, state elements can be combined into state

cells, which are multiplied into state arrays, which in turn may be grouped together to form state engines." Consider further for example page 9, lines 18-25, which states

> Increasing the total state storage volume by multiplying State Cells can also increase overall state access bandwidth as the throughput of an individual State Cell is likely to be a little lower than that of the interconnect. If the number of State Cells is increased to the point that the interconnect becomes the limiting factor then aggregate throughput can be further increased by providing multiple interconnect channels, each channel accessing a different portion of the array (ie. table). This is analogous to designing a memory system with multiple, independently addressable channels to increase random access bandwidth.

Accordingly, it is respectfully submitted that the "wherein said state engine includes a plurality of state elements which comprise a plurality of local shared memories which provides a composite bandwidth that is a sum of all bandwidths associated with each one of said plurality of local shared memories" is supported in the originally filed specification.

As regarding Claim 43, consider for example page 9, lines 28-30. That section states in relevant part that "[t]he State Engine combines State Arrays with all the additional glue logic and facilities that are required to construct a block which can be configured and accessed via a system bus." Accordingly, it is respectfully submitted that "wherein state transactions are processed with said state engine and accesses to shared memory are passed on a system bus" is supported in the originally filed specification.

As regarding Claims 44-46, consider for example pages 4-5, lines 31-4. That section states

> State Elements are the key components in the present context which perform the serialisation of accesses into a shared memory. In the context of parallel processors, where simultaneous access to shared state is increasingly likely, there are potentially many state elements all in parallel, executing function calls from the parallel processors but instead of it all being SIMD, where the parallel processors are operating from a single instruction stream, the state elements operate in parallel but from individual instruction streams. They effectively operate in response to requests from processors.

Accordingly, it is respectfully submitted that "wherein each of said plurality of state elements includes a single serialization access point resulting in a plurality of serialization access points within said state engine" and "wherein said plurality of state elements perform as a plurality of partitioned processing functions" are supported in the originally filed specification. Further, it is respectfully submitted that "a plurality of state engines, wherein one or more of said state engines are applied to a system bus and wherein said one or more of said state engines operate separately from each other" is also supported in the originally filed specification.

For at least the above reasons, reconsideration and withdrawal of the rejection of claims 39-46 are respectfully requested.

Claims 19-40 were rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Steely, Jr. et al. (U.S. Patent No. 6,088,771, herein "Steely") in view of Dieffenderfer et al. (U.S. Patent No. 5,822,608, herein "Dieffenderfer").

Claim 41 was rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Steely in view of Dieffenderfer, and further in view of Tetrick (U.S. Patent Publication No. 2001/0021967, herein "Tetrick"). As noted above, during the interview of October 23, 2009, a clarifying claim amendment was discussed and was indicated as overcoming the applied art rejections. That amendment is herein made to Independent Claims 19, 32, 35, 36, and 38. Specifically, Independent Claims 19, 32, 35, 36, and 38 have been amended to more clearly recite that the recited request includes at least a command directing said at least one state element means on how to perform an operation on said shared state, and that said operation includes reading, modifying, and writing back said shared state. It is respectfully submitted that at least pages 6-7, lines 29-15 of Applicant's originally filed specification supports this feature.

In addition to the arguments presented in the last response, all of the outstanding rejections of the claims on the merits are respectfully traversed for at least the following reasons.

Briefly recapitulating, independent Claim 19 is directed to a state engine that receives multiple requests from a parallel processor for a shared state. The state engine includes at least one state element means, the at least one state element means adapted to operate, atomically, on the shared state in response to a request made by the parallel processor. The request includes at least a command directing the at least one state element means on how to perform an operation on the shared state. The operation includes reading, modifying, and writing back said shared state. The state

engine also includes a memory connected to the at least one state element means and configured to store the shared state.

The claimed one state element unit advantageously achieves, for example, faster access for the parallel processor to the shared state, as shown for example in Figure 5(b) of the present application and its corresponding description in the specification.

Turning to the applied art, Steely discloses a technique that reduces a latency of a memory barrier operation used to impose an inter-reference order between sets of memory reference operations issued by a processor to a multiprocessor system having a shared memory. More specifically, Figure 2 shows a local switch 200 communicating with a plurality of processors P1 to P4 such that inputs from the processors are serialized before being sent to a shared memory 150. Figure 2 shows that the switch 200 includes an arbiter 240 that arbitrates, among input queues from the processors P1 to P4, to grant access to the Arb bus 170, where the requests are ordered into a memory reference request stream. The arbiter 240 selects the request stored in the input queues for access to the bus in accordance with an arbitration policy, such as a conventional round-robin algorithm, as disclosed in Steely in the paragraph bridging columns 6 and 7.

Thus, the device of Steely does not teach or suggest that a request from any of the processors P1 to P4 includes at least a command directing the arbiter 240 regarding how to perform an operation (i.e., reading, modifying, and writing back said shared

state) on the shared memory 150, as recited, among other things, by the independent claims.

In other words, the arbitration system of Steely does not perform an operation on the shared memory 150 based on a command from the processors P1 to P4 but rather acts based on the round-robin algorithm, which is not provided by the processors P1 to P4. Steely simply queues and arbitrates updates to memory from the processors and does not teach or suggest processors sending commands to the state engine directing it regarding how to update the memory.

In this regard, if a processor in Steely needs to increment a shared memory location, then the processor needs to read the data from the memory, increment the value, write it back to the memory, and then issue a memory barrier instruction to synchronize this update with all the other processes. However, this operation delays the other processors from accessing that memory location until the first processor has finished the complete sequence read-modify-write operation, as illustrated in Figure 5(b).

To the contrary, the claimed invention avoids this latency because any number of state processors may instruct the state engine via the requests, for example, to increment the same shared state and the processors may immediately continue with other processing. Thus, the processors do not have to wait for the whole operation read-modify-write to be performed, as illustrated by Figure 5(a).

Dieffenderfer and Tetrick have been considered but do not cure the deficiencies of Steely discussed above with regard to independent Claim 19.

Accordingly, reconsideration and withdrawal of the rejections of claims 19-41 under 35 U.S.C. § 103(a) over Steely in view of Dieffenderfer, and over Steely in view of Dieffenderfer and Tetrick are respectfully requested.

All of the objections and rejections raised in the outstanding Office Action having been addressed, it is respectfully submitted that this application is in condition for allowance and a notice to that effect is earnestly solicited. Should the Examiner have any questions regarding this response or the application in general, she or he is invited to contact the undersigned at (540) 361-1863.

Respectfully submitted,

POTOMAC PATENT GROUP PLLC

By: /stevenmdubois/
Steven M. duBois
Registration No. 35,023

Date: October 26, 2009

Potomac Patent Group PLLC
P.O. Box 270
Fredericksburg, VA 22404
(540) 361-2601